REMARKS

Claim 21 is amended to render it more definite and certain and is not amended to reduce the scope of claim so as to avoid reading on prior art cited by the Examiner. All claims are therefore intended to be broadly interpreted to cover all modes of practicing the invention employing the combination of elements as recited in any one of the claims, including modes employing elements that are functional equivalents of those described in the specification.

The following numbered sections of these remarks are provided in response to similarly numbered sections of the office action.

1 (a).

The applicant has argued that HAYASHI fails to disclose the "base IC die", the "first secondary IC die" or the "conductive contacts" but the Examiner disagrees with the arguments. However the applicant's arguments in this regard are correct and the Examiner's rebuttal fails to overcome them for the reasons stated below.

The "Base IC Die"

Claim 21 recites four elements: a substrate, a base IC die, a first secondary IC die and conductive contacts. It is not clear from the Examiner's comments which elements of HAYASHI's FIGs. 1 and 3 the Examiner considers to correspond to four elements of the applicant's claim 21.

Does the Examiner consider item 1 to be the "substrate" or the "base IC die"? He refers to item 1 as being both things.

Does the Examiner consider item 1 or item 5 to be the "substrate"? He refers to both items as being "the substrate".

Does the Examiner consider items 3 to be the "base IC die" or the "secondary IC die"? The Examiner clearly considers items 3 to be "IC die" but it is unclear as to whether he considers them the "first secondary die", "the base IC die", or both.

It is therefore difficult for the applicant to respond to the Examiner's rebuttal to the applicant's arguments without making some assumptions as to what the Examiner's position is with respect to the correspondence between elements of claim 21 and elements HAYASHI's FIGs. 1 and 3 since the Examiner's positions are unclear and to some extent self-contradictory. However for purposes of providing a

response, the applicant will assume the Examiner's position with respect to three of the four elements of claim 21 is as follows:

a. the "substrate" reads on PCB 5,

b. the "first secondary IC die" reads on any one of devices 3, and

c. the "conductive contacts" read on terminals 4.

Now the applicant must make an assumption as to what the Examiner's position is regarding the fourth element of claim 21, the "base IC die", in a manner that is consistent with the above assumptions a-c. The Examiner has accused hybrid IC 1 of being the "base IC die" but he has also accused it of being the "substrate". Since the applicant has assumed that the Examiner considers PCB 5 to be "the substrate", then the applicant cannot now assume that the Examiner intended hybrid IC 1 to be "the substrate" without violating assumption (a).

Does the Examiner then intend hybrid IC 1 to be the "base IC die"? That is one of his two opinions of what hybrid IC 1 might be, but this opinion conflicts with assumptions a-c. Since HAYASHI (column 4, lines 40-50) tells us that hybrid IC 1 includes devices 2, 3 and 4, then given assumptions a-c above, at most only a part of hybrid IC 1 can be "base IC die" since assumptions a-c designate portions hybrid IC as being other things.

Which element of FIGS. 1 and 3 could possibly be the considered the "base IC die" given assumptions a-c? Let us first eliminate from consideration all elements of FIGs 1 and 3 for which our assumptions a-c have already assigned another role. We therefore eliminate items 3 because they are assumed to be the "first secondary die", and we eliminate terminals 4 because they are assumed be the "conductive contacts". We also eliminate item 5 because that is assumed to be the substrate. Thus we are left only items 2, 2a, 4A, 4b and 6 as possible candidates for being the "base IC die".

Since HAYASHI describes item 2 as a "circuit board" (column 4, line 42), the Examiner clearly could not consider item 2 to be the "base IC die" since one of skill in the art would confuse and an IC die with a circuit board.

Since HAYASHI describes items 2a as "electrodes" (column 4, line 50), the Examiner clearly could not be considering items 2a to be the "base IC die" since one of skill in the art would not confuse an IC die with an electrode.

Since HAYASHI describes items 4a and 4b as "plates" that are part of terminals 4 (column 4, lines 56-60), the Examiner clearly could not be considering items 4a and 4 b to be the "base IC die", since one of skill in the art would not confuse a plate portion of a terminal with an IC die.

That leaves only item 6. HAYASHI does not tell us what item 6 is, but it does not appear to be an IC die and nothing in HAYASHI suggests that item 6 might be the "base IC die". Possibly item 6 is intended to be solder for connecting terminal 4 to circuit boards 2 and 5 because column 5, line 1-5 mention that the terminals 4 are soldered to electrodes 2a. In any case, it does not seem reasonable to assume that one of skill in the art would consider items 6, whatever they may be, to be the recited "base IC die".

At this point we have run out of reasonable candidates for the "base IC die" given assumptions a-c above. Could one of those assumptions be wrong? Perhaps the Examiner actually does consider hybrid IC 1 to be the "base IC die", which is indeed one of his two stated views as to what element of claim 21 hybrid IC 1 might be. However one of skill in the art would not consider a hybrid circuit of the type taught by HAYASHI to be the same thing as an IC die. An IC die (or "chip" as the Examiner calls it) is a piece (usually a thin rectangle) of semiconductor material that has been doped to form devices such as transistors and the like therein and which usually includes layers of insulating and conducting material formed on top of the semiconductor material to provide signal paths between the circuit devices formed within the material. HAYASHI does not describe hybrid IC 1 as being such a thing. HAYASHI describes it as being a combination of a circuit board 2, some electronic components 3, and some terminals 4. Given HAYASHI's description of hybrid IC 1, and the generally accepted meaning of the term "IC die", no one of skill in the art would confuse hybrid IC 1 with an IC die.

Thus from the above discussion, regardless of whatever the Examiner's position is with respect to the "base IC die" recited in

the applicant's claim 21, HAYASHI fails to teach the recited base IC dic.

The "Secondary Die"

The applicant assumed that the Examiner considers items 3 is to be the recited "first secondary die". Is this correct? HAYASHI calls them only "electronic elements" but does not indicate in any further detail what kind of elements they are. Given that the Examiner is rejecting claims under 37 CFR 102, the fact that HAYASHI does not directly indicate elements 3 are or could be die arguably renders the rejection under section 102 invalid. The fact that the Examiner suppose items 3 might be IC die is irrelevant and insufficient grounds for sustaining a section 102 rejection insofar as the Examiner's suppositions are not prior art.

In any case, elements 3 do not look like IC die because IC die do not have little legs (presumably conductors of some sort) extending from their edges as shown in FIGs 1 and 3. Signal connections to an IC die are provided at conductive pads formed on the wide top surface of dic, not along its edges. See for example, the applicant's FIG. 4 which shows solder ball conductors 83 contacting pads 81 on the top of die 85. Thus if one of objects 3 were an IC die, as the Examiner suggests, the little conductors would be shown as contacting the planar top surface of the object (or the bottom surface if the die were flipped over), rather than contacting its narrow edge surfaces.

Of course since they look remarkably like packaged ICs, it is possible that one of skill in the art might guess that one or more of items 3 could in fact be a packaged IC. A typical packaged IC includes a die hiding somewhere inside a package (a little plastic box, usually black), a set of conductive pins extending through the package walls, and tiny bond wires inside the package connecting terminals on a surface of the IC die to the package pins. However even though it is possible that one or more of items 3 might be a packaged IC including a die inside a package, nothing in HAYASHI would lead one of skill in the art to assume that any one of items 3 is itself an IC die. The depictions of them in FIGs. 1 and 3 lead one away from that conclusion.

In any case, let us assume that there is a die inside one of items 3. Could such a die be the "first secondary die" recited in

claim 21? Looking more closely at claim 21 we find a limitation on the first secondary die; it must reside between the base IC die and the substrate. Thus the "first secondary IC die" of claim 21 would read on an IC die that might be hiding inside one of items 3 only if the hidden die resides between another IC die ("the base IC die") and a "substrate". We see from FIG. 3 that any IC die that might reside within one of items 3 would reside between two circuit boards, 2 and 5, but we do not see it as residing between a substrate and another (base) IC die as recited in claim 21. As discussed above, we never found a base IC die in FIGs. 1 and 3. Hence even if we assume that HAYASHI teaches that a die resides inside one of items 3 (and HAYASHI clearly does not teach that), HAYASHI does not teach the recited position limitations on that die, namely that it reside between a base IC die and a substrate. Hence HAYASHI fails to teach the recited "first secondary die".

The "Conductive Contacts"

We assumed above that the Examiner considers terminals 4 to be the "conductive contacts" recited in calm 21. Is this correct? Clearly they are conductive and clearly they contact things, so they clearly can be considered to be "conductive contacts". But claim 21 includes an additional limitation on the conductive contacts beyond being conductive and beyond being contacts. Claim 21 recites that the conductive contacts must extend between a first surface of the base IC and conductors on the substrate. We have established above that a base IC does not exist in HAYASHI's FIGs. 1 and 3. Therefore it is not possible for terminals 4 to extend between a base IC die and a substrate. Moreover, from FIG. 3 we can see clearly that terminals 4 extend between a substrate 4 and electrodes 2a on another substrate 2. FIGs. 1 and 3 thus teach away from the recited conductive contacts. Since terminals 4 do not meet the limitation on the conductive contacts recited in claim 21, HAYASHI fails to teach the recited "conductive contacts."

Thus the applicant's argument (a) that HAYASHI fails to disclose the "base IC die", the "first secondary IC die" and the "conductive contacts" is correct, and the Examiner's rebuttal to the argument is overcome.

1(b).

The applicant has argued that HAYASHI teaches "electronic elements" but does not teach they are IC die. In rebuttal, the Examiner states that "the electronic components (3) typically is integrated circuit chips or IC chips which is consider as IC dies (for other terminology term)". However HAYASHI does not refer to items 3 as being anything other than "electronic elements" and never calls them "die", "dies", "chips" or any other synonym for an IC die. By the way they are drawn in FIGs. 1 and 3, no one of skill in the art would be led to conclude items 3 are IC die since, as discussed above, no IC die has terminals on its narrow edges as shown in FIGs. 1 and 3. One of skill in the art might at best consider devices 3 to be packaged ICs, though electronic devices other than ICs are packaged in a similar manner. Accordingly FIGs. 1 and 3 teach away from the notion of items 3 being IC die. Thus applicant's argument (b) is correct; HAYASHI teaches "electronic elements" but does not teach they are IC die.

1(d).

The applicant has argued that HAYASHI fails to teach "solder forms the first conductive signal paths" as recited in claim 22. The Examiner rebuts the argument by stating that HAYASHI teaches contacts 4 are soldered to electrodes 2a. However the "conductive signal paths" are recited in parent claim 21 as extending between a base IC die and conductors on a substrate. In HAYASHI's FIG. 1 the signals paths 4 extend between a substrate 5 and conductors 2a on another substrate 2. As discussed above, there is no base IC <u>die</u>. Hence HAYASHI discloses no signal path between a substrate and a base IC die as recited in claim 22. Also HAYASHI fails to disclose a "solder" signal path. Item 6 of FIG. 3 is apparently solder, but it does not provide a signal path between a die and a substrate. Solder 6 provides a path from PCB 5 to terminal 4. Solder 6 also provides a signal path between terminal 4 and PCB 2. Thus the applicant's argument (d) is correct; HAYASHI fail to teach "solder forms the fist conductive signal paths".

1(e).

The applicant has argued that HAYASHI fails to teach the substrate is a semiconductor substrate as recited in claim 24. Since the Examiner does not present any rebuttal to this argument other than to say the "Examiner disagrees", the applicant is unable to comment on whatever reason the Examiner may have had for disagreeing with the applicant's argument. As discussed in the applicant's prior response, nothing in HAYASHI mentions anything about PCB 5 being a semiconductor substrate. He calls it a printed circuit board (column 5, lines 28-34.) Item 2 is also called a circuit board (column 4, line 43). Those of skill in the art do not confuse printed circuit boards with semiconductor substrates. Hence HAYASHI teaches away from use of semiconductor substrates. Therefore the applicant's argument (e) is correct; HAYASHI fails to teach the substrate is a semiconductor substrate.

1(f).

The applicant has argued that HAYASHI fails to teach "second secondary IC die links by second conductive paths to the second surface of the base IC die" as recited in claim 29. Claim 29 is supported by the applicant's FIG. 11. The "second secondary die" reads on die 220 or 221 which is linked to the second (top) surface of base die 212. Claim 29 recites, as shown in FIG. 11, a base die 212 with first and second secondary die connected to both its top and bottom surfaces. Nothing in HAYASHI even remotely looks like FIG. 11. The Examiner rebuts the applicant argument by stating that items 3 could be the "second secondary IC die". But items 3 cannot be either the first secondary die or the second secondary die because they aren't die and they aren't connected through signal paths to a base IC die. Also claim 29 recites that the first and secondary die are linked to <u>different</u> surfaces of something, and regardless of what kind of thing 2 items 3 are linked to through signal paths, they are linked to the <u>same</u> surface of thing 2, not different surfaces. Hence the applicants argument (f) was correct; HAYASHI does indeed fail to teach "second secondary IC die linked by second conductive paths to the second served of the base IC die".

With respect to the 37 CFR 102 rejection of claim 30, the

Examiner has failed to rebut the applicant's argument with that HAYASHI fails to teach the recited conductive vias.

2,3.

Claims 21-24 and 29-30 continue to be rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,569,952 (HAYASHI). Since the Examiner's explanation for the rejection of these claims appears to be identical to the explanation provided in the office action dated 4/25/2002, the applicant's arguments provided in the response to that office action, and the remarks in section 1 above overcoming the Examiner's rebuttal to those arguments serve to distinguish each one of these claims over HAYASHI. The Examiner is therefore respectfully requested to withdraw the rejection of claims 21-24 and 29-30.

4,5.

Claims 25-28 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,330,164 (HAYASHI), in view of U.S. Patent 6,330,164 (KHANDROS). Since the Examiner's explanation for the rejection of claims 25-28 and 31 appears to be identical the explanation provided in the office action dated 4/25/2002, the applicant's arguments provided in the response to that office action, and the remarks in section 1 above overcoming the Examiner's rebuttal to those arguments serve to distinguish each one of these claims over HAYASHI.

Claim 30 is newly rejected over the combination of HAYASHI and KHANDROS. The Examiner cites KHANDROS FIGS. 2 and 4B as showing vias 23 or 23A providing signal paths between first and second surfaces of a die 12 as recited in claim 30, however neither of items 23 and 23A is a via passing though die 12. KHANDROS (column 12, lines 42-45) describes item 23A as being a "terminal" raised from the surface of die 12. KHANDROS (column 12, lines 64-66) describes item 23 as being a "terminal". FIG. 2 clearly depicts terminals 23 and 23A as residing on a lower surface of die 12. Perhaps the Examiner mistook for vias the lines in FIG. linking the reference character "23A" to the rectangles depicting terminals 23A.

In view of the foregoing arguments against rejection of claims 25-28 and 30-31, the Examiner is respectfully requested to withdraw the rejection.

It is believed that in view of the foregoing amendment and remarks, the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Charles A. MILLER

Art Unit: 2827

Application No: 09/970,749

Examiner: Tuan T. Dinh

Filed: October 3, 2001

For: MULTIPLE DIE INTERCONNECT SYSTEM

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 21, rewrite as follows:

21. (Amended) A multiple die electronic system comprising:

a substrate having conductors formed thereon,

a base IC die having a first surface facing the substrate and a second surface parallel to the first surface,

a first secondary IC die residing between the first surface of the base IC die and the substrate and linked to the first surface of the base IC die through first conductive signal paths, and

conductive contacts extending between the first surface of the base IC die and the conductors on the substrate for conveying signals between the base IC die an the conductors on the substrate.